FIG. 4 is a diagram showing an exemplary function block structure of the display terminal;

FIG. 5 is a diagram showing exemplary encoding processing section and clock generation section of the base device;

FIG. 6 is a diagram showing exemplary decoding processing section and clock generation section of the display terminal;

FIG. 7 is a diagram illustrating a synchronization method of the present invention;

FIGS. 8A and 8B are diagrams both illustrating the synchronization method of the present invention;

FIG. 9 is a diagram showing an exemplary clock frequency control routine to be executed by a control section at a decoder end;

FIG. 10 is a diagram showing another exemplary clock frequency control routine to be executed by the control section at the decoder end;

FIG. 11 is a diagram illustrating a synchronization method in an MPEG-2 system;

FIGS. 12A to 12D are diagrams all illustrating a case where jittering occurs in a transmission path; and

FIGS. 13A to 13E are diagrams all illustrating a case of using a timestamp for the transmission path.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(Summary of System Embodiment : FIGS. 1 to 4)

As an embodiment of the present invention, described